AMENDMENTS TO THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (Currently amended) A monitoring device integrated on a chip of a microprocessor executing a sequence of instructions, comprising:

a message calculation means for, on each execution of an instruction from among a plurality of instructions of predetermined instruction types, generating a digital message of a type from a plurality of types corresponding to the executed instruction, wherein [[a]] the type of the digital message corresponds to a type of the executed instruction;

a buffer memory of the monitoring device for storing each generated digital message; and

a plurality of output terminals connected to an external analysis tool, ~~at least one~~ each output terminal from the plurality of output terminals being associated with an instruction type from among the instruction types, wherein, simultaneously with storing in the buffer memory, at a storage time, of a digital message of a type from the plurality of types, the type corresponding to the instruction type associated with an output terminal from the plurality of output terminals, the storage time is provided to the external analysis tool by modifying ~~the message calculation means modifies~~ a state of the ~~at least one~~ output terminal ~~substantially simultaneously with storing in the buffer memory, at a storage time, a digital message of a type corresponding to the instruction type associated with the at least one output terminal~~ to ~~indicate to the external analysis tool the storage time~~.

2. (Previously presented) The monitoring device of claim 1, wherein the buffer memory is divided into a plurality of areas, each of the areas is associated with a different instruction type and is intended to only store digital messages associated with said instruction type.

3. (Previously presented) The monitoring device of claim 1, wherein each output terminal is connected to a test terminal.

4. (Previously Presented) The monitoring device of claim 1, wherein each output terminal is connected to an input terminal of a coding block comprising a predetermined number of coding block output terminals, each of the coding block output terminals is connected to a test terminal, each coding block being provided to have each of its n coding block output terminals switch once every n state switchings of its input terminal and so that a single one of its n coding block output terminals switches state at once.

5. (Previously Presented) The monitoring device of claim 1, wherein only certain types of instructions are associated with an output terminal of the message calculation means.

6. (Previously presented) The monitoring device of claim 1, wherein each of the predetermined instruction types is associated with an output terminal of the message calculation means.

7. (Currently amended) An integrated circuit comprising:

a microprocessor for executing a sequence of instructions; and

a monitoring device for monitoring the execution of the sequence of instructions, the monitoring device comprising:

a message calculation means for generating digital messages of a plurality of types, wherein a type from the plurality of types of each digital message corresponds to a predetermined type of an instruction from a plurality of predetermined instruction types, and wherein the digital message of the type is generated on each execution of the instruction of the predetermined type;

a buffer memory for storing the generated digital messages; and

a plurality of output terminals connected to an external analysis tool, wherein an output terminal from the plurality of output terminals is associated with an instruction type, and wherein, simultaneously with storing in the buffer memory, at a storage time, of a digital message of a type from the plurality of types, the type corresponding to the instruction type associated with an output terminal from the plurality of output terminals, the storage time is provided to the external analysis tool by modifying ~~the message calculation means modifies~~ a

state of the ~~at least one~~ output terminal ~~substantially simultaneously with storing in the buffer memory, at a storage time, a digital message of a type corresponding to the instruction type associated with the at least one output terminal~~ to ~~indicate to the external analysis tool the storage time~~.

8. (Currently amended) A method for monitoring a microprocessor executing a sequence of instructions by means of a device integrated to a microprocessor chip, the method comprising:

on each execution of an instruction from the sequence of instructions, generating a digital message of a type corresponding to a type of the executed instruction;

storing each generated digital message in a buffer memory; ~~and~~

simultaneously with storing in the buffer memory, at a first storage time, a first digital message of a first type corresponding to an instruction type associated with a first output terminal from a plurality of output terminals connected to an external analysis tool, providing the first storage time to the external analysis tool by modifying a state of [[an]] the first output terminal; and

simultaneously with storing in the buffer memory, at a second storage time, a second digital message of a second type corresponding to an instruction type associated with a second output terminal from the plurality of output terminals, providing the second storage time to the external analysis tool by modifying the state of the second output terminal so that the external analysis tool determines a time elapsed between storing at the first storage time of the first digital message and storing at the second storage time of the second digital message.

~~associated with an instruction type from the sequence of instructions substantially simultaneously with storing in the buffer memory, at a storage time, a digital message of a type corresponding to the instruction type, wherein the output terminal associated with the instruction type is from a plurality of output terminals connected to an external analysis tool, with each output terminal from the plurality of output terminals being associated with an instruction type from the sequence of instructions.~~

9. (Previously Presented) The method of claim 8, wherein the buffer memory is divided into a plurality of areas, with each area from the plurality of areas storing digital messages associated with an instruction type.

10. (Previously Presented) The integrated circuit of claim 7, wherein the buffer memory is divided into a plurality of areas, with each area from the plurality of areas storing digital messages associated with an instruction type.

11. (Currently amended) The integrated circuit of claim 7, wherein each output terminal is connected to a test terminal, the test terminal couples the output terminal to the external analysis tool.

12. (Previously Presented) The integrated circuit of claim 11, wherein a state of the test terminal is modified when a state of the output terminal connected to the test terminal is modified.

13. (Previously Presented) The integrated circuit of claim 7, wherein, when at least two instructions of a first and a second type from the sequence instructions are executed in parallel, the message calculation means generates a digital message corresponding to an instruction of a first type and modifies a state of an output terminal associated with the instruction of the first type and simultaneously generates a digital message corresponding to an instruction of a second type and modifies a state of an output terminal associated with the instruction of the second type.

14. (Canceled)

15. (Previously Presented) The integrated circuit of claim 7, wherein each output terminal is connected to an input terminal of a coding block comprising a predetermined number of coding block output terminals, each of the coding block output terminals is connected to a test terminal, wherein a state of a coding block output terminal switches once per the predetermined

number of times a state of the input terminal switches, and wherein the predetermined number of the coding block output terminals switch states one at a time.

16. (Previously Presented) The integrated circuit of claim 7, wherein each output terminal from the plurality of output terminals is associated with a plurality of instruction types.

17. (Previously Presented) The integrated circuit of claim 7, wherein each instruction type is associated with an output terminal.

18. (Previously presented) The monitoring device of claim 1, wherein

the plurality of output terminals are connected to the external analysis via a plurality of test terminals,

each output terminal from the plurality of output terminals is connected to a test terminal from the plurality of test terminals, and

a state of the test terminal is modified when a state of the output terminal connected to the test terminal is modified.

19. (Previously presented) The monitoring device of claim 1, wherein, when at least two instructions of a first and a second type from the sequence instructions are executed in parallel, the message calculation means generates a first digital message corresponding to an instruction of a first type and modifies a state of an output terminal associated with the instruction of the first type substantially simultaneously with storing the first digital message in the buffer memory and simultaneously generates a second digital message corresponding to an instruction of a second type and modifies a state of an output terminal associated with the instruction of the second type substantially simultaneously with storing the second digital message in the buffer memory.

20. (Previously presented) The method of claim 8, wherein

the plurality of output terminals are connected to the external analysis via a plurality of test terminals,

each output terminal from the plurality of output terminals is connected to a test terminal from the plurality of test terminals, and

a state of the test terminal is modified when a state of the output terminal connected to the test terminal is modified.